IN THE SPECIFICATION

Replace the paragraph beginning at page 5, line 8 with the following rewritten paragraph:

In Fig. 1 a communications system includes a transmitter (Tx) 10 for transmitting a signal (u), the transmitter 10 having an inner FEC encoder 12, a FEC interleaver 14, an outer FEC encoder 16 outputting an encoder signal (c), a channel interleaver 18 and a digital modulator 20. The output of the digital modulator 20 ~~(signal (x)~~(signal (x)) is transmitted through a channel 22 and is received as signal (y) at a receiver (Rx) 24 having a corresponding digital demodulator 26, a channel de-interleaver 28 that outputs a signal (Lc) and a concatenated FEC decoder 30. Further downstream circuitry is not shown, as it is not germane to an understanding of this invention.

Replace the paragraph beginning at page 14, line 18 with the following rewritten paragraph:

Fig. 13 shows an embodiment of a block SNR estimator and erasure insert circuit 48 that is suitable for use with turbo decoding. The signal y received from the channel 22 is applied to the input of a 1:L multiplexer (MUX) 70, which outputs y(k) to y(k+L-1) symbols in parallel to a SNR estimator 72. The output of the SNR estimator is applied to a comparator 74 that compares the estimated SNR of L symbols to the SNR threshold (T). T will typically have a value < 0dB, and may be fixed or programmable (variable). The binary output (0/1) of the ~~comparator 78~~comparator 74 is applied as a control input to an output symbol multiplexer 78 the outputs either the received symbol stream, via pipeline delay 76 (L symbols in duration), or a zero symbol, to the FEC decoder (e.g., 58) or channel de-interleaver 28, depending on how the receiver is architected.